WHAT IS CLAIMED IS:

1. A circuit for distributing a clock signal in an integrated circuit having a plurality of metal layers therein, comprising:

a capacitive clock distribution circuit having at least conductor therein; and

at least one inductor formed in a metal layer of the integrated circuit, said inductor being coupled to said at least one conductor and having an inductance value selected to resonate with the capacitive clock distribution circuit.

2. The circuit for distributing a clock signal, as defined by claim 1, wherein the at least one conductor in the clock distribution circuit includes a clock grid.

3. The circuit for distributing a clock signal, as defined by claim 2, wherein the at least one conductor in the clock distribution circuit further includes a tree distribution circuit coupled to the clock grid.

4. The circuit for distributing a clock signal, as defined by claim 3, wherein the integrated circuit has a plurality of operating sectors and wherein the at least one conductor further comprises a tree distribution circuit corresponding to each of the sectors of the integrated circuit.

5. The circuit for distributing a clock signal, as defined by claim 1, wherein the at least one inductor includes a plurality of inductors distributed on the clock distribution circuit.

6. The circuit for distributing a clock signal, as defined by claim 5, wherein the plurality of inductors take the form of spiral inductors.

7. The circuit for distributing a clock signal, as defined by claim 6, further comprising a plurality of decoupling capacitors formed in the integrated circuit, the plurality of decoupling capacitors corresponding to the plurality of spiral inductors, wherein the spiral inductors are coupled to a power-ground grid potential in the integrated circuit by a corresponding decoupling capacitor.

8. The circuit for distributing a clock signal, as defined by claim 1, further comprising a decoupling capacitor formed in the integrated circuit, wherein the at least one inductor is coupled to a power-ground grid potential by a coupling capacitor formed in the integrated circuit.

9. A circuit for providing a clock signal in an integrated circuit comprising:

a clock driver circuit, the clock driver circuit providing a clock signal having a clock frequency;

a clock distribution circuit having at least one conductor therein, the clock distribution circuit being coupled to the clock driver circuit; and

a plurality of inductors coupled to the clock distribution circuit, the plurality of inductors being spatially distributed about the clock distribution circuit and presenting a total inductance value which is substantially resonant with the clock distribution circuit at the clock frequency.

10. The circuit for providing a clock signal, as defined by claim 9, wherein the at least one conductor in the clock distribution circuit includes a clock grid.

11. The circuit for providing a clock signal, as defined by claim 10, wherein the at least one conductor in the clock distribution circuit further includes a tree distribution circuit coupled to the clock grid.

12. The circuit for providing a clock signal, as defined by claim 11, wherein the integrated circuit has a plurality of operating sectors and wherein the at least one conductor further comprises a tree distribution circuit corresponding to each of the sectors of the integrated circuit.

13. The circuit for providing a clock signal, as defined by claim 12, wherein the clock driver circuit includes a plurality of buffer amplifiers, wherein each tree distribution circuit corresponding to a sector is coupled to at least one of the plurality of buffer amplifiers.

14. The circuit for providing a clock signal, as defined by claim 13, wherein the clock distribution circuit includes at least a further tree distribution circuit, said further tree distribution circuit being coupled to the buffer amplifiers in a plurality of sectors of the integrated circuit.

15. The circuit for providing a clock signal, as defined by claim 12, wherein the clock driver circuit comprises a plurality of phase lock loop circuits, wherein each tree distribution circuit corresponding to a sector is coupled to at least one of the plurality of phase lock loop circuits.

16. The circuit for providing a clock signal, as defined by claim 9, wherein the plurality of inductors take the form of spiral inductors.

17. The circuit for providing a clock signal, as defined by claim 16, further comprising a plurality of decoupling capacitors formed in the integrated circuit, the plurality of decoupling capacitors corresponding to the plurality of spiral inductors, wherein the spiral inductors are coupled to a power-ground grid potential in the integrated circuit by a corresponding decoupling capacitor.

18. The circuit for providing a clock signal, as defined by claim 17, wherein a voltage potential at the junction of a spiral inductor and corresponding decoupling capacitor is provided as a reference voltage for psuedodifferential switching of the clock signal.

19. The circuit for providing a clock signal, as defined by claim 9, further comprising at least one capacitor switchably coupled to the clock distribution circuit, whereby the total capacitance of the clock distribution circuit can be tuned by switching said at least one capacitor.

20. A method of distributing a clock signal in an integrated circuit having at least one clock distribution conductor therein, comprising:

determining the capacitance of clock distribution conductor and circuitry coupled thereto;

determining the inductance value required to resonate with the capacitance at a clock frequency; and

coupling at least one inductor to said clock distribution conductor to provide said inductance value.